ABSTRACT OF THE DISCLOSURE

An apparatus, in a data processing system having at least one host processor with host processor cache and host memory, includes a chip interconnect, a cache coherent interface coupled to the chip interconnect wherein the cache coherent interface provides cache coherent access, a cache non-coherent interface coupled to the chip interconnect wherein the cache non-coherent interface provides cache non-coherent access to the host memory, and a compute engine coupled to the chip interconnect and coupled to the cache coherent interface and coupled to cache non-coherent interface wherein the compute engine issues a memory access request. Other methods and apparatuses are also described.